what is claimed is :

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1. A semiconductor device having an input/output protection circuit section on a semiconductor substrate; wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first and second diffusion layers of first conductive type and a gate electrode that is set in the region sandwiched between these layers; and

a dopant diffusion region of second conductive type is set at a distance from the region where said plurality of field effect transistors are formed; and

while said dopant diffusion region is connected with a reference potential, the second diffusion layer is connected with an input/output terminal section; and

under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

2. The semiconductor device according to Claim 1, wherein said gate electrode and said dopant diffusion region of second conductive type are placed over the second conductive type well that is formed on the surface of the semiconductor substrate; and the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level

deeper than the bottom of the second conductive type well.

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3. The semiconductor device according to Claim 1, wherein said field transistors are N-channel type field effect transistors.

4. A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section that contains a complementary field effect transistor; wherein:

said complementary field effect transistor is composed of a first field effect transistor having a first and second diffusion layers of first conductive type and a gate electrode that is set in the region sandwiched between these layers and a second field effect transistor having a third and fourth diffusion layers of second conductive type and a gate electrode that is set in the region sandwiched between these layers; and

a first dopant diffusion region of second conductive type is set at a distance from the region where said first field effect transistor is formed, and a second dopant diffusion region of first conductive type is set at a distance from the region where said second field effect transistor is formed; and

the first dopant diffusion region is connected with a first reference potential; the second dopant diffusion region, with a second reference potential; and the second

diffusion layer and the fourth diffusion layer are each connected with an input/output terminal section; and

under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

5. The semiconductor device according to Claim 4, wherein the gate electrode of the first field effect transistor and the first dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate; and the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

6. The semiconductor device according to Claim 5, wherein, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well; and the bottom of said first conductive type well is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

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7. The semiconductor device according to Claim 4, wherein the first field transistor is an N-channel type field effect transistor.

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